WHAT IS CLAIMED IS:

1. A method of handling a plurality of instructions within a processor comprising:

loading the plurality of instructions into a register;

determining the number and size of the plurality of instructions; and

decoding the plurality of instructions.

2. The method of Claim 1, further comprising decoding the plurality of instructions within a single clock cycle.

3. The method of Claim 1, further comprising decoding the plurality of instructions substantially simultaneously.

4. The method of Claim 1, further comprising decoding width bits to determine the size of the instructions.

5. The method of Claim 1, further comprising communicating the number and size of the plurality of instructions to the decoder.

6. The method of Claim 1, further comprising loading a first of the plurality of instructions having a first size and a second of the plurality of instructions having a second size.

7. The method of Claim 6, further comprising loading a first of the plurality of instructions having a first size, and loading a second and a third of the plurality of instructions having a second size, wherein the first size is 32-bits and the second size is 16-bits.

8. The method of Claim 1, handling the plurality of instructions within a digital signal processor.

9. A method of decoding a plurality of instructions within a processor comprising:

determining the size of the plurality of instructions;

presenting the plurality of instructions from an instruction register to a decoder; and

decoding each of the plurality of instructions within a single clock cycle.

10. The method of Claim 7, further comprising simultaneously presenting each of the plurality of instructions to the decoder.

11. The method of Claim 7, further comprising pre-decoding the plurality of instructions to determine the width of the plurality of instructions.

12. The method of Claim 7, further comprising loading a next plurality of instructions into the single instruction register.

13. The method of Claim 9, further comprising decoding a plurality of instructions in a digital signal processor.

14. A processor comprising:

an instruction register capable of holding a plurality of instructions;

a pre-decoder which determines the size and number of the plurality of instructions; and

a decoder which substantially simultaneously receives the plurality of instructions from the instruction register, wherein the decoder decodes each of the plurality of instructions within a single clock cycle.

15. The processor of Claim 14, wherein the pre-decoder determines width bits.

16. The processor of Claim 15, wherein the pre-decoder receives information from each instruction source.

17. The processor of Claim 14, wherein the pre-decoder communicates the number and size of the plurality of instructions to the decoder.

18. The processor of Claim 14, wherein the processor is a digital signal processor.

19. An apparatus, including instructions residing on a machine-readable storage medium, for use in a machine system to handle a plurality of instructions, the instructions causing the machine to:

determine the size of the plurality of instructions;

present the plurality of instructions from an instruction register into a decoder; and

decode each of the plurality of instructions within a single clock cycle.

20. The apparatus of Claim 19, wherein each of the plurality of instructions is simultaneously presented to the decoder.

21. The apparatus of Claim 19, wherein the size of the plurality of instructions is determined from width bits.

22. The apparatus of Claim 19, wherein a next plurality of instructions is loaded into the single instruction register.